RESEARCH ARTICLE

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Enhancement of Power Quality with Increased Levels of Multi-level Inverters in Smart Grid Applications

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Abstract

Research focuses on renewable energy-based smart grids to meet appropriate energy demands in a world where climate change and power management are becoming more significant. The smart grid is a modernized autonomous power network that can efficiently transmit electricity, save money and resources, and improve the stability of the local grid. As a result, a multi-level inverter (MLI) that is connected to the smart grid is provided in this work. To meet the requirements of the smart grid network, the inverter is controlled using a model predictive control algorithm with increased levels with the main objectives of controlling the injected power generated by the renewable source, improving the quality of the current waveform, lowering THD, and eliminating the shift phase between the current and the grid voltage.

Keywords: Inverter, Multilevel Inverters, Predictive Control, Renewable Energy, Smart Grid.

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Introduction

Power electronics inverters are increasingly more widely used for several applications, such as clean energy, electric power systems, and motor drive systems (renewable). Due to their numerous advantages, such as high-quality output waveforms, less voltage stress on switches, decreased switching losses, and better efficiency, multilevel inverters have also recently attracted a lot of attention. The idea behind multilevel inverters (MLIs) is to convert power utilizing minuscule voltage increases by using many semiconductor switches. These MLIs have been widely employed in high or medium power operations, including variable-speed drives as well as static VAR compensator (SVC) reactive power compensation.[1] MLIs also were applied to low-power operations like solar power systems (PV) and hybrid e-mobiles. The neutral point clamped (NPC), recently developed flying capacitor (FC), and to produce inverted AC from separate DC sources the cascaded H-bridge (CHB), these considered as 3 fundamental topologies of MLI. The fundamental drawback of the NPC inverter is unmatched voltage sharing among series capacitors, which causes grossly imbalanced DC-link capacitance and necessitates extra clamping diodes.[2] Recently developed Flying capacitors are used as clamping diodes in the FC inverter. Compared to NPC inverters, this design provides several benefits, including equivalent voltage sharing across semiconductor switches. Such kind of topology, however, necessitates a large quantity of storage capacitors for high voltage steps. The cascaded H-bridge CHB inverters are made up of H-Bridge cells that are coupled in series including an isolated dc supply. That topology is appropriate for high-level operations because of its versatility and ease of handling. Depending upon the values by dc voltage supply VS, the CHB inverters split into 2 major sections: symmetric and asymmetric topologies. The symmetric topology employs equal-valued dc input VS like battery or generator. This characteristic provides high modularity by giving only some levels as in output waveform compared to asymmetric one, which uses various dc VS to provide increased output voltage levels [3]-[5]. Multilevel inverters biggest drawback is the enormous amount of switches needed. As a result, much work has gone into developing novel MLI topologies with fewer power semiconductor devices (or say switches). A novel topology implementing cascaded Multilevel inverters was described in other research.[6] MLI's novel design for a fuel-cell microgrid system includes a transformer-free 5-level MLI. To create five levels, a simplified Multilevel inverters suggested[7] employs just 6 power semiconductor devices (or switches)

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of the 8 utilized in a standard cascaded H-Bridge MLI. The mentioned topology, however, necessitates using a step-up converter (DC to DC power convertor) and a combination of Inductor and capacitor L-C filter. As growing output levels, several different topologies have been created to decrease usage of switches necessary.

Related Works

Some researcher has[8] improved 13-level framework and analysis of PUC-MLI is suggested in this work. The suggested inverter employs 8 switches device and 3 Voltage sources to eliminate harmonic, effectively controlled SPWM method. The resultant currents and voltages were examined, revealing that the MI is dependable and performs well. To reduce undesirable harmonic, an LPF filter is built into the MI output. The suggested inverter has a low harmonic distortion, which results in great power quality and a compact frequency response. Due to their many benefits over conventional MI, this are getting prominence attention for usage in a spectrum of uses. This study presents a 13-level smooth waveforms as the output of a modified PUC-MI. In comparison to traditional MI. The proposed inverter employs just 8 switching devices and 3 DC sources. To examine the results of the designed MI , simulations are run by using Matlab/Simulink program. The improved output waveform and decreased THD are highlighted, demonstrating the suggested PUC-MI efficiency. Proposed 13-level having 8 switching IGBT's are in operation. The output voltage's THD is 10% without utilizing any harmonics filters. It's 0.05 percent after filtration. For the applicability of distributing generated systems, in [9] author proposed a novel single-phase DC-AC MI based on cascaded transformers MLI(CTMLI). 19-level voltage output synthesizing are used to validate the suggested CTMLI procedure. The suggested inverter reduces THD to 5.607% up to 500 kHz without a filter, and to 3.08% with a filter. The suggested work uses a 7 level, 19, 37 level output with 8,12, and 16 number of switches. Utilizing 9, 13 and 17-level MLI topologies, in other study,[10] author offered a redesigned MLI architecture. A HRES is constructed coupled to a redesigned Cascaded Half-Bridge Multi Level Inverter (CHB-MLI), with switching driven by an ANN model. The suggested hybrid renewable energy method includes ten Metal (MOSFETs) with 17 levels. With minimal components and lower THD, the suggested architecture works well . The suggested system's CHB- MLI performance is evaluated by creating a methodology in the MATLAB/ SIMULINK environment. To demonstrate the efficacy of the suggested model, the simulated performance of the suggested CHB-MLI for the renewable energy application is evaluated and the results of current models were discussed. For 17 level MLI has ten MOSFET switching devices. The THD rate is reduced to 3.58%. In a research,[11] author proposed design has a lower number of Dc voltage sources, switches, component count level factor, lower TSV, greater effective, lower THD, and is less expensive than existing Proposed topology. The 9 and17-level MLIs are also investigated with various cascaded load. The suggested inverter is robust under non-linear loading condition and is well suited for grid-connected FACTS and sustainable energy uses. THD is 8.49% for 9 level with 7 switches and 4.12% for 17 levels with 12 switches, respectively. The 9th and 7th levels are 95 and 92% efficient, respectively. In a study,[12] author designed and tested a grid-connected solar energy conversion system based on a binary hybrid MLI. Ten semiconductor switches and three binary weighted isolated DC-sources make up the 15 level BHMLI. At dynamic load and PV changes, balanced, sinusoidal, and in-phase grid currents are obtained. As a result, SECS operation maintains grid power quality within IEEE-519 guidelines. 1.35% is the computed THD. In[13] proposed a microprocessor-based digital output. Besides, Pseudo Random Multi-Carrier (PRMC) involves two random PWM strategies to minimize the harmonic order for 9- a level cascaded multilevel H-bridge (CHB) inverter and a 9-level Modular Multilevel inverter are introduced. In[14] author proposes a three-phase hybrid cascaded modular Multi - level inverter architecture based on a modified H-bridge modules is suggested in this study. In comparison to traditional CHB and flying capacitance (FC), the FC has fewer switches, lower capacitor requirements, and lower VBC. When compared to a three phase 9-level cascaded H-bridge Inverter, it lowers switch count by 50%, gate drive demand by 43.75%, and energy source requirement by 58.33%. In a study,[15] author presented in this study an asymmetrical cascaded H-bridge MLI for solar systems. Under the level shifted modulation approach, the output voltage vs. time plot displays a THD of 3.84% spectrum. In a study,[16] author proposed 11-level multilevel inverter prototype. To achieve Nstep for the load, the proposed architecture requires minimal switches and gate driver circuits with low standing voltage on switching devices. In a study,[17] The response time of the PI and FLC controllers for a Photovoltaic seven level MLI a three-phase induction generator was investigated in this research. Two distinct controllers are used to assess the motor's efficiency. The FLC outperforms the PI controller in terms of rising time , error, THD as well as output waveform quality. As a result, the FLC with seven multi-level inverters generates a better output than the traditional PI controller. The THD is 17.04% with a frequency of 19.29 Hz as a result. In a study,[18] a novel MLI architecture for a three-phase grid-connected solar (PV) system is proposed in this research. In comparison to typical symmetric MLIs, the suggested symmetric MLI creates seven levels with fewer power switches. The suggested architecture is simulated, and the modification of capacitor voltages, inverter output voltage, and grid-injected current are provided to evaluate the proposed seven-levels MLI's performance. The proposal has a Harmonic distortion of 3.28%, according to the results. In a study,[19] author created a novel cascaded asymmetric MLI for solar electricity production with fewer switching circuitry. There are three main sources plus 11 switching devices in

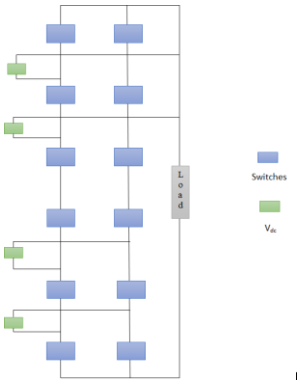

Figure 1: MLI's Power Circuit Diagram

the circuit. The cascaded structure›s voltage THD is 0.34%, while the current THD is 0.13%, both of which are within IEEE519 harmonic standards. In a study,[20] author proposed an advanced MLI circuit to reduce The suggested circuit's functioning and sequence of operations are explained and demonstrated. To create the power circuits' controlling pulses innovative various carrier controlling technique is applied in the elements. THD was 1.89% and requires 16 switches.

System Description and Principle of Operation

Figure 1 depicts the power circuit of the MLIs. Only *N* unidirectional switches, *N* diodes, with *N/3* asymmetric dc supply are used by the suggested approach. The essential DC sources are separated and can be provided by renewable energy sources like photovoltaics and fuel cells. The suggested MLI focuses on lowering MLI complexities with optimizing output voltage levels in order to enhance power quality. The amount of unidirectional switches (control a current in one direction only), bidirectional switches (services in both directions), or power amplifier like gate drivers, capacitors (2-terminal, electrical component), as well as DC sources all have a role in mitigating the MLI's complexities. By earlier analysis, the no. of the symmetric level for given MLI (N_{level}) can be written as this equation:

$$N_{level}=2\left(\frac{Vdc1+Vdc2+Vdc3+Vdc4}{Vdc1}\right)+1 \qquad (i)$$

This classification of MLI, a simplest approach, is employed to generate pulses. As illustrated in Figure 2, such approach comprises of 4 phases: reference sine-wave signal, for compares two voltages or currents using comparators, logic circuits (electric circuit), and driving circuits to generate appropriate pulses for the switches.

The reference signal (RS) is split by same amount of levels as the output waveform's levels required. The peak value (V_p) and the number of levels requested (N) define the values of the voltage step (V_{step}) of the RS as follows:

$$V_{step}=\frac{2Vp}{N-1} \qquad (ii)$$

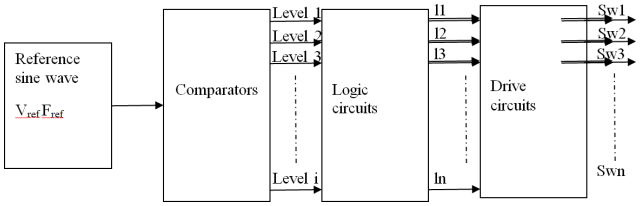

Figure 2: Switching pulse system phases

The voltage level (V_i) written as; considering positive half cycle:

$$V_i == (i -- 1) * V_{step} \qquad (iii)$$

Here, I = order of level and variation from 0 to (N+1)/2

To avoid DC coefficient of output waveform, for other negative half cycle having equal voltage level , difference is that it is of a negative value.

Within that procedure, the switching angles are determined using a comparator. The switching instants are generated by comparison of the reference signal to critical levels. The critical value is where the reference sine wave transitions from one level on to another. It's set as the halfway point between the 2 levels to guarantee of output waveform, resulting in a wave having little numbers of harmonics. The comparator switch's critical values were evaluated as follows:

$$V_{cri}==\frac{V_i+V_{i+1}}{2} \qquad (iv)$$

Here, (i) == order of the level.

Result Analysis

In this section, implementation details about results and discussion of this research work. In this section, performance evaluation platform, performance evaluation parameters as well as result analysis is discussed. MATLAB was used as an implementation platform for the proposed architecture. Table 1 shows the parameters description with their values including resistance, Inductance, Capacitance, DC voltage, Frequency, Load type and levels.

Figure 3 and 4 shows output variable with the switching variable to generate 7 levels output and Output voltage generated for 7-level MLI. In comparison to the present approach, the suggested method produces more precise

Table 1: Parameters Description

Input Parameters	*Values*
Resistance	1 ohm
Inductance	2e-3 H
Capacitance	1e-3 F
DC voltage	220 volt
Frequency	50Hz
Load Type	Resistance
Levels	7–27

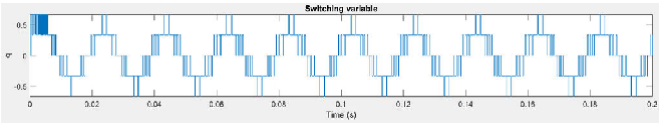

Figure 3: Switching Variable to generate 7 level output

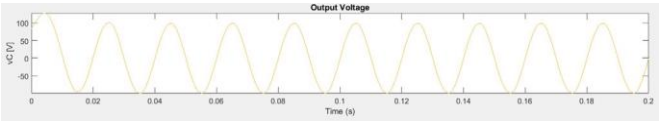

Figure 4: Output voltage generated for 7-level MLI

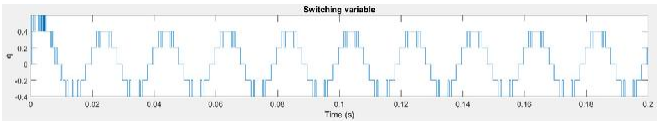

Figure 5: Switching Variable to generate 11 level output

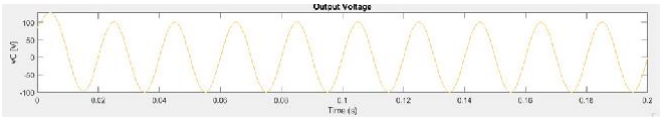

Figure 6: Output voltage generated for 11-level MLI

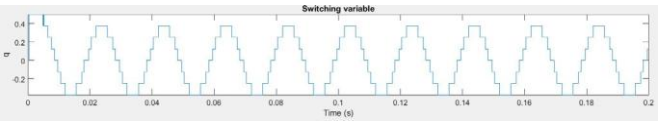

Figure 7: Switching Variable to generate 17 level output

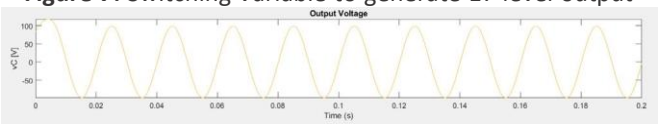

Figure 8: Output voltage generated for 17-level MLI

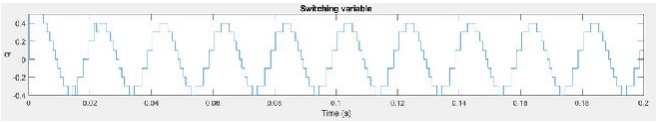

Figure 9: Switching Variable to generate 21 level output

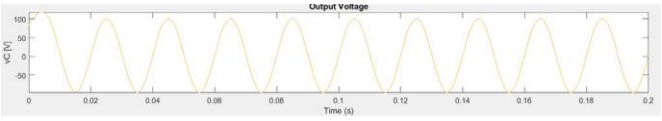

Figure 10: Output voltage generated for 21-level MLI

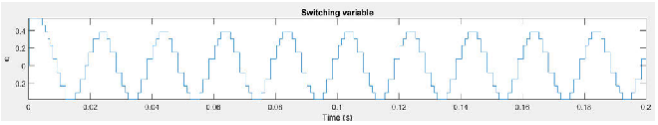

Figure 11: Switching Variable to generate 27 level output

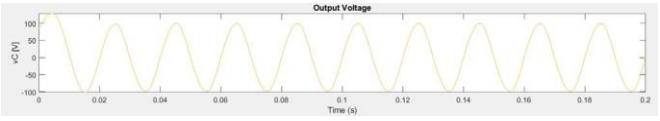

Figure 12: Output voltage generated for 27-level MLI

sinusoidal output with varying time between 0 to 0.2 seconds. Figure 5 shows the output voltage created for 11-level MLI with varying duration between 0 to 0.2 second and Figure 6 shows output variable with switching variable to generate 11 level output. Figure 7 shows output variable with the switching variable to generate 17 level output and Figure 8 shows the Output voltage generated for 17-level MLI with varying time between 0 to 0.2 seconds. Figure 9 shows output variable with the switching variable to generate 21 level output and Figure 10 shows the Output voltage generated for 21-level MLI with varying time between 0 to 0.2 seconds. Figure 11 shows output variable with the switching variable to generate 27 level output and Figure 12 shows the Output voltage generated for 27-level MLI with varying time between 0 to 0.2 seconds.

Table 2: THD Analysis with variable levels

MLI levels	*THD (in dB)*	*THD (in %)*
Level 7	-43.56	0.663
Level 11	-44.33	0.607
Level 17	-46.2	0.499
Level 21	-36.53	1.49
Level 27	-33.14	2.20

Table 2 shows THD analysis with the variable levels, THD in dB and percentage as well. Level 7 has THD -43.56 dB and 0.663 in % . Whereas Level 11 has slightly lower THD -44.33dB and 0.607 %. Level 17 has -46.2 THD in dB and 0.499 in %. Level 21 has -36.53 dB and 1.49 THD in percentage. Level 27 has highest THD around - 33.14 dB and 2.20%.

Conclusion

In this study, an MLI with more levels is created and applied to smart grid applications for renewable energy. The fundamental advantage of the MLI family is that it addresses the problems of total harmonic distortion, EMI, and switch stress. More devices based on NLI topologies are becoming accessible in the industrial or commercial industries. Still, research is being done on layout complexity and control circuits. The main issue with the majority of MLIs is that if the switching control is not built appropriately, total harmonic distortion (THD) will increase as the level is raised. Therefore, in this research predictive control is done on renewable energy-based smart grid inverters to improve level with minimum THD.

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